Remarks

Claims 1-19, as amended, are pending in this application. Claim 1 has been amended to further clarify what is meant by the terms "superficial zone" and the "holes or voids" which were previously identified as "pitting." In particular, the superficial zone is now defined to have a thickness of less than about 100 nm while the small holes or voids are defined as having a size of a few nm in depth and a few dozen nm in diameter. Support for these changes is provided in the specification, wherein the thickness of the superficial layer is recited in the first paragraph of the Detailed Description on page 6 and the definition of the holes or voids is found on the last paragraph on page 3. Claim 15 has been amended to recite that it is the superficial layer that is converted to oxides and removed. Support for this change can be found at the last full paragraph at page 9. As no new matter has been introduced, the entry of this amendment is warranted at this time. In particular, these claim amendments should be entered to reduce the issues for an appeal by placing the application in condition for allowance.

In the final office action, claims 1, 3-13, 15-16 and 18-19 were again rejected for allegedly being anticipated by Aga et al., U.S. Patent No. 6,372,609 ("Aga"). The issue appears to be that the claims are considered to encompass the process of Aga. Applicants submit that this rejection is in error.

Claim 1 pertains to a method for preparing a semiconductor wafer, which includes removing a superficial zone of defined size that is supported by a wafer before conducting rapid thermal annealing to prevent formation of holes or voids of defined size in the surface of the wafer during a subsequent rapid thermal annealing treatment. As previously explained, the superficial zone has a thickness of less than 100nm and the small holes or voids would otherwise form in the superficial zone of the wafer surface during the rapid thermal annealing step if the superficial zone is not removed.

Applicants have previously explained that the term "pitting" is used differently in the prior art in general and in the Aga patent in particular to describe holes or defects that are embedded in the thickness of the wafer material. The current specification goes to great lengths to establish this difference, but to avoid any incorrect interpretation, claim 1 has been now amended to recite the size of the holes that are eliminated by applicants' process. In this regard, applicants' process eliminates the superficial zone in which these holes are found after rapid thermal annealing to thus facilitate the final processing steps of the wafer surface.

In contrast, as previously explained, the methods disclosed by Aga are directed to removing a much greater amount of surface material to remover larger defects that are encountered after a rapid thermal annealing treatment. In particular, the Aga patent discloses that the resultant SOI layer 7 can include defects such as COPs (Crystal Originated Particles) that extend to the oxide film 3 under the damaged layer of silicon and which are not eliminated, and are sometimes enlarged, by heat treatment at a high temperature for an extended period of time. When this occurs, the buried oxide layer 3 may be etched by hydrogen or the like seeping in through defects to form etch pits that cause problems because the SOI layers near them are affected by them (see Aga, col. 2, lines 37-49 and Fig. 1E). Accordingly, an object of Aga is to provide a method of fabricating an high quality SOI waver using a hydrogen ion delamination method, wherein the at least the entire damaged layer present on the surface of the SOI layer after delamination, and usually a greater thickness than that layer, is removed, resulting in a uniformly thick SOI layer (see Aga, col. 2, lines 58-65). To achieve the stated object, Aga teaches to form an oxide film on an SOI layer by heat treatment in an oxidizing atmosphere after a bonding heat treatment, removing the oxide film, and then subsequently heat treating in a reducing atmosphere (col. 2, line 66 to col. 3, line 5 and Figs. 1G to 1I). When the oxide film is formed, all or a part of the damage layer on the surface of the SOI layer is incorporated therein, so that when the oxide layer is removed (Fig. 1H), all of the damaged layer is removed. When the SOI layer is subsequently subjected to heat treatment in a reducing atmosphere, none of the damaged layer remains on the SOI layer so that surface roughness is improved.

Aga does not suggest or teach to remove only a superficial zone of less than 100 nm prior to conducting rapid thermal annealing to prevent the formation of small holes or voids in the wafer surface during the rapid thermal annealing as recited in claim 1. Furthermore, Aga's treatments are intended to remove much greater thicknesses of material. Col. 10, lines 16-20 describe that the damaged layer resulting after treatment has a thickness of 150nm and that pits deeper that 150 nm are observed. Thus, as noted in col. 10, lines 35-42, Aga performs an oxidation treatment to form an oxide layer having a thickness of 340 nm, i.e., twice (or more) the thickness of the damaged layer, so that all of the damaged layer and any COPs or pits can be removed.

Removing a greater thickness of surface layer can be problematic as the removal of large defects by oxidation can expose the underlying oxide layer. Then during the

subsequent rapid thermal annealing, these exposed area can be etched or damaged (see col. 2, lines 36-49). In contrast, the present invention removes a much smaller thickness of surface layer, i.e., less than 100 nm, so that the underlying oxide layer is protected and not subject to damage from the rapid thermal annealing step.

The present invention, as defined in claim 1, is distinguishable from Aga for at least two reasons, namely, that the process is conducted to remove the relatively thin superficial layer of 100 nm or less, and that the process is conducted prior to rapid thermal annealing to avoid forming small holes or pits in the surface of the wafer during that step. Thus, claim 1 is not anticipated by Aga. Since claims 2-19 all directly or indirectly depend on claim 1, these claims also are not anticipated. In view of the above remarks, the applicant respectfully requests withdrawal of the 35 U.S.C. 102(e) rejections of the claims.

Claim 2 was rejected for allegedly being unpatentable over Aga in view of admitted prior art, while claim 14 was rejected for allegedly being unpatentable over Aga in view of Nakashima et al., U.S. Patent No. 5,989,981 and claim 17 was rejected for allegedly being unpatentable over Aga in view of Park et al., U.S. Patent No. 6,566,198.
As these claims all depend from claim 1, and since the secondary references do nothing to remedy the deficiencies of the Aga patent, these rejections should be withdrawn.

In view of the above remarks, the applicants respectfully submit that the entire application is in condition for allowance, early notice of which would be appreciated. Should the Examiner not agree that all pending claims are allowable, then a personal or telephonic interview is respectfully requested to discuss any remaining issues and expedite the eventual allowance of these claims.

Respectfully submitted,

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